

JFET Voltage-Controlled Resistors

Product Summary

Part Number	V _{GS(off)} Max (V)	V _{(BR)GSS} Min (V)	r _{DS(on)} Max (Ω)
VCR2N	-7	-25	60
VCR4N	-7	-25	600
VCR7N	-5	-25	8000

For applications information see AN105.

Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance

Benefits

- Gain Ranging Capability/Wide Range Signal Attenuation
- No Circuit Interaction
- Simplified Drive

Applications

- Variable Gain Amplifiers
- Voltage Controlled Oscillator
- AGC

Description

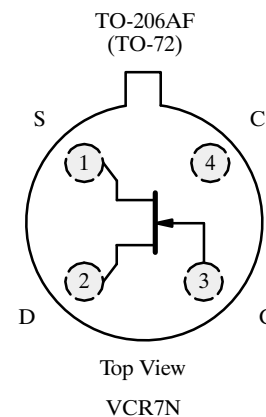
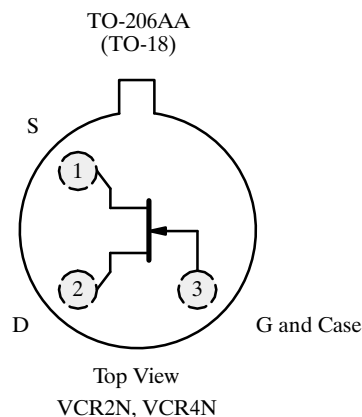
The VCR2N/4N/7N JFET voltage controlled resistors have an ac drain-source resistance that is controlled by a dc bias voltage (V_{GS}) applied to their high impedance gate terminal. Minimum r_{DS} occurs when V_{GS} = 0 V. As V_{GS} approaches the pinch-off voltage, r_{DS} rapidly increases. This series of junction FETs is intended for applications where the drain-source voltage is a low-level ac signal with no dc component.

change versus V_{GS} bias where:

$$r_{DS\text{bias}} \approx \frac{r_{DS}(@ V_{GS} = 0)}{1 - \left| \frac{V_{GS}}{V_{GS(off)}} \right|}$$

Key to device performance is the predictable r_{DS}

These n-channel devices feature r_{DS(on)} ranging from 20 to 8000 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500 (see Military Information).



Absolute Maximum Ratings^a

Gate-Source, Gate-Drain Voltage -25 V
 Gate Current 10 mA
 Power Dissipation^b 300 mW
 Operating Junction Temperature Range -55 to 175°C
 Storage Temperature -65 to 200°C

Lead Temperature (¹/₁₆" from case for 10 sec.) 300°C

- Notes:
 a. T_A = 25°C unless otherwise noted.
 b. Derate 2 mW/°C above 25°C.

VCR2N/4N/7N

Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit
				VCR2N		VCR4N		VCR7N		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-55	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10 V, I_D = 1 \mu A$		-3.5	-7	-3.5	-7	-2.5	-5	
Gate Reverse Current	I_{GSS}	$V_{GS} = -15 V, V_{DS} = 0 V$			-5		-0.2		-0.1	nA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, I_D = 10 mA$		20	60					Ω
		$V_{GS} = 0 V, I_D = 1 mA$				200	600			
		$V_{GS} = 0 V, I_D = 0.1 mA$						4000	8000	
Gate-Source Forward Voltage	$V_{GS(F)}$	$V_{DS} = 0 V, I_G = 1 mA$	0.7							V
Dynamic										
Drain-Source On-Resistance	$r_{ds(on)}$	$V_{GS} = 0 V, I_D = 0 mA$ $f = 1 kHz$		20	60	200	600	4000	8000	Ω
Drain-Gate Capacitance	C_{dg}	$V_{GD} = -10 V, I_S = 0 mA$ $f = 1 MHz$			7.5		3		1.5	pF
Source-Gate Capacitance	C_{sg}	$V_{GS} = -10 V, I_D = 0 mA$ $f = 1 kHz$			7.5		3		1.5	

Notes:

a. $T_A = 25^\circ C$ unless otherwise noted.

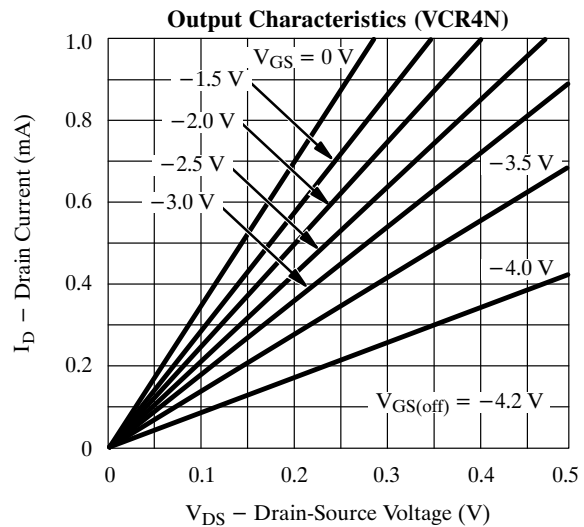
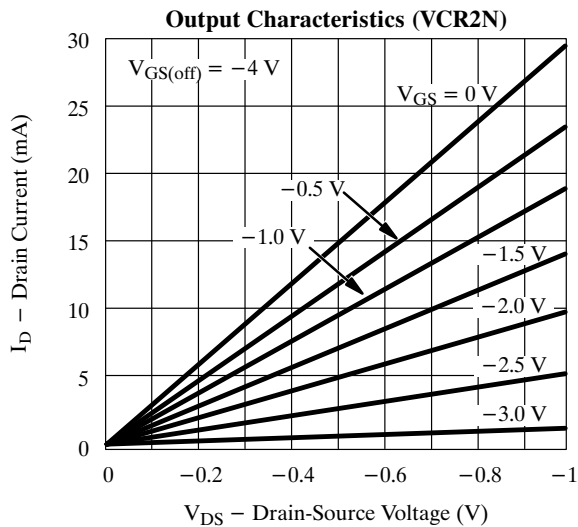
NCB

NPA

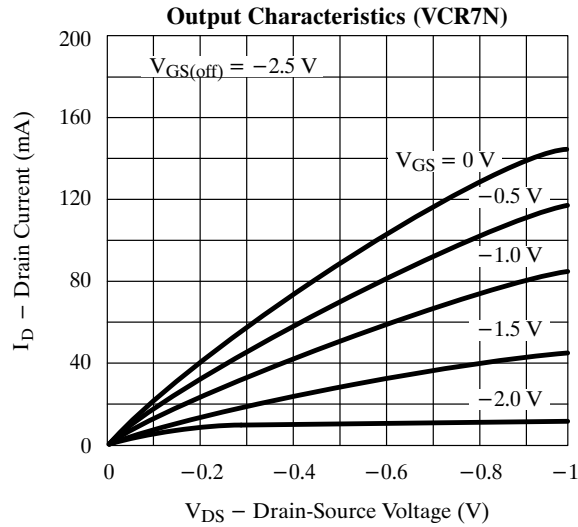
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b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Characteristics



Typical Characteristics (Cont'd)



Applications

A simple application of a FET VCR is shown in Figure 1, the circuit for a voltage divider attenuator.

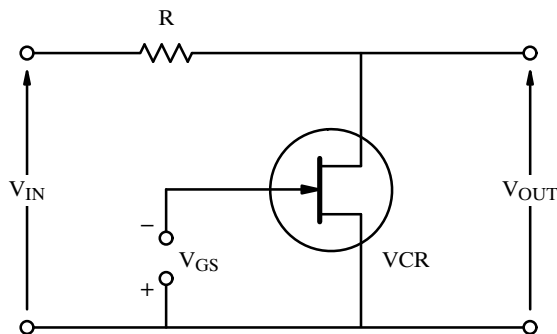


Figure 1. Simple Attenuator Circuit

The output voltage is:

$$V_{OUT} = \frac{V_{IN} r_{DS}}{R + r_{DS}}$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which V_{OUT} can assume is:

$$V_{OUT(min)} = \frac{V_{IN} r_{DS(on)}}{R + r_{DS(on)}}$$

Since r_{DS} can be extremely large, the highest value is:

$$V_{OUT(max)} = V_{IN}$$